Recommended Practice for Hardware Analysis for Vital Electronic/Software-Based Products Used in Safety-Critical (Vital) Applications

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A. Purpose

This Manual Part recommends hardware analysis requirements to be used as part of the analysis of vital electronic/software based products and systems used in safety-critical (vital) applications.

B. General

1. This Manual Part contains a recommended list of failure modes which should be considered in the safety analysis of vital electronic/software based products and systems used in safety-critical (vital) applications.

2. The program described in this Manual Part should be considered a guideline to Manufacturers and Railways involved in the development, manufacturing and utilization of vital electronic/software based products and systems used in safety-critical (vital) applications.

C. Reference Documents

1. Manual Part 17.1.1 Definitions of Terms Used in the Manual Parts in Section 17.

2. Manual Part 17.3.1 Recommended Safety Assurance Program for Vital Electronic/Software-Based Products Used in Safety-Critical (Vital) Applications.

3. Manual Part 17.4.1 Recommended Reliability and Maintainability Assurance Program for Vital Electronic/Software-Based Products Used in Signal Applications.

4. ANSI/IEEE Standard 1483-2000 Standard for the Verification of Vital Functions in Processor-based Systems Used in Rail Transit Control.

5. CENELEC EN50129 Railway Applications - Communication, Signalling and Processing Systems – Safety Related Electronic Systems for Signalling.

6. IEC 60384-14 Fixed capacitors for use in electronic equipment – Part 14: Sectional specification – Fixed capacitors for electromagnetic interference suppression and connection to the supply mains.

7. CENELEC EN 50205 Relays with forcibly guided (mechanically linked) contacts.

8. CENELEC EN 50124-1 Railway applications - Insulation coordination - Part 1: Basic requirements - Clearances and creepage distances for all electrical and electronic equipment

D. Abbreviations

FMECA Failure Modes Effects and Criticality Analysis

PFU Probability of a Failure Being Unsafe

WCA Worst Case Analysis

CENELEC European Committee for Electrotechnical Standardization

E. Hardware Design Requirements

1. CLASS I Hardware (Vital Hardware)

   a. Vital hardware circuits shall be designed to enable exhaustive and comprehensive analysis using failure modes, effects, and criticality analysis (FMECA) techniques.

2. CLASS II Hardware (Non-vital Hardware Used to Implement Vital Functions)

   a. Hardware designated as CLASS II hardware shall be designed such that all credible failures, including secondary failures in combination with non-self-revealing initial failures, within that hardware shall be demonstrated, by analysis and/or tests, to either:

      (1) Have no unsafe effect on the implementation of vital functions; or

      (2) Be detected and, once detected, subsequent action shall assure that no unsafe effect is produced. In this case, the detection of failures that could have an unsafe effect shall be accomplished by continually proving that the failure has not occurred.

   b. Functional Fault Trees (FFT) may be used to identify those failures that must be considered in CLASS II Hardware at a functional block level.

3. CLASS III Hardware (Hardware not used for Vital Functions)

   Hardware not used for the implementation of vital functions and not designated as either CLASS I, or CLASS II hardware shall be designated CLASS III.

a. CLASS III hardware shall be designed so that it can be demonstrated that operation of or failure within that hardware has no effect on the safe implementation of vital functions.

4. Implementation of vital hardware shall specifically include separation of PCB traces and components, detailed specification of components, and the separation and demarcation between CLASS I, CLASS II and CLASS III circuits.

F. Analysis of CLASS I Hardware

1. An FMECA is required on all hardware designated as CLASS I (vital hardware). The minimum requirements of the FMECA are:

   a. All credible failure modes of all components shall be analyzed and/or tested by being induced or simulated on the physical hardware circuit, fabricated in final form. Simulation or engineering analysis may be used where physical testing is destructive or not achievable.

      (1) Component and circuit failure modes analyzed in the FMECA shall include as a minimum those specified in minimum requirements for the FMECA of CLASS I Vital Hardware below (Section I).

   b. The FMECA shall classify all failure modes as either self-revealing or non-self-revealing.

   c. The FMECA shall show that no single failure mode produces an unsafe condition.

   d. The FMECA shall show that all first level non-self-revealing failures in combination with subsequent failures produce no unsafe conditions. Engineering judgment shall be used to determine if additional level failures should be considered.

G. Analysis of CLASS II Hardware

1. An analysis shall be provided, at the functional block level, showing that all possible failures of CLASS II hardware which could adversely affect the safe implementation of vital functions have been accounted for by showing that either:

   a. the failure will have no unsafe effect on the implementation of vital functions, or

   b. the failure will be detected and once detected, subsequent action assures that no unsafe effect is produced.

2. The types of analyses provided depend upon the safety assurance concepts used, the system design, and the factors upon which safety assurance is dependent. The following requirements apply in providing analyses depending upon system design and factors on which safety assurance is dependent.

   a. Designs Incorporating Self-Checking

      In those systems in which safety assurance is dependent upon the identification of all failure modes and the effects of their occurrence being anticipated, the analysis shall show:

      (1) All credible failures that could adversely affect the safe implementation of a vital function have been anticipated. Functional Fault Trees as described in IEEE 1483-2000 may be used to identify the credible failures.

      (2) Any mechanism or test designed to detect the occurrence of each failure is effective in revealing the failure.

      (3) The reaction of the system, once the failure is revealed, maintains a safe state or states.

      (4) The mechanism or test used to reveal the failure and the subsequent system reaction to the occurrence of the failure cannot be compromised by the failure itself, or any subsequent failure or combination of failures, or by unrevealed errors in the software.

   b. Designs Incorporating Checked Redundant Comparison

      In those systems in which safety assurance is dependent on hardware failures being revealed by comparison of independent hardware circuits, the analysis shall show:

      (1) All credible failures that could adversely affect the safe implementation of vital functions are revealed by detecting differences in the points of comparison between the systems. Functional Fault Trees as described in IEEE 1483-2000 may be used to identify the credible failures.

      (2) The comparison mechanism has no mode of failure that could compromise its ability to detect differences between the systems.

      (3) The reaction of the system, once the failure is revealed, maintains a safe state or states.

(4) The mechanism or test used to reveal the failure and the subsequent system reaction to the occurrence of the failure cannot be compromised by the failure itself, or any subsequent failure or combination of failures, or by errors in the software.

c. Designs that Incorporate Numerical Assurance Techniques

The analysis of those systems in which safety is assured by the guarantee of an upper bound on the PFU shall show:

(1) The method used to calculate the PFU is valid and the calculations are accurate.

(2) All ancillary functions required to be performed for the PFU to be considered valid are performed correctly.

(3) All factors upon which the validity of the PFU depends are complete and correct.

(4) The mechanism and techniques used to verify numerical results are such that failures cannot reduce the value of the PFU of the processor-based system in which it resides. All failures that could adversely affect the safe implementation are included in the numerical coverage. Functional Fault Trees as described in IEEE 1483-2000 may be used to identify the credible failures.

H. Analysis of CLASS III Hardware

An analysis shall be provided proving that operation of or failure within that hardware designated as CLASS III hardware within the system has no effect on the safe implementation of any vital function.

I. Minimum Requirements for the Failure Modes and Effects Criticality Analysis of Vital Hardware

1. As a minimum, the following failure modes and conditions shall be analyzed in the FMECA performed on all hardware designated as CLASS I hardware:

a. Circuit operational modes not necessarily related to component failures, such as self-oscillation, acceptance of spurious signals, vulnerability to electrical or mechanical shock, and any phenomena that may mimic signals normally indicating safe conditions, shall be analyzed.

b. Further, the effects of variations in power supply voltages, switching transients and ripple, and possible coupling of circuits through common power supplies shall be analyzed.

c. Filters shall be analyzed to show that undesired signals are prevented from passing through the filter at levels that could cause unsafe conditions, even in the event of component failures within the filter.

d. Sneak circuit paths, particularly those caused by components and/or wires connected to a common or grounded node, must be considered.

e. Multiple faults occurring from a common cause are considered a single failure. Potential common causes shall be considered to provide assurance that multiple faults occurring as a result of a common cause, are safe.

2. Component Failure Modes

a. All failure modes listed could be intermittent. Intermittent failures are caused by environmental influences such as temperature variation or mechanical stress (relevant environmental conditions per Manual Part 11.5.1 Recommended Environmental Requirements for Electrical and Electronic Railroad Signal System Equipment). Therefore, the frequency of intermittent failures will be in accordance with these causes (factors).

b. The following list of failures represents the MINIMUM analysis that shall be performed. CENELEC 50129 may be used as a reference to consider additional failure modes.

c. Component failure modes shall be analyzed individually and shall include the following:

Those failure modes marked with (*) below, can be included in the analysis as non-credible ONLY for the special components and under the specific conditions as described in section I.2.e.(3).

Those failure modes marked with (**) below can be justified in the analysis as non-credible provided the items in I.2.e.(1) are satisfied. The considerations described in Section I.2.e.(4) may be used as part of that justification.

(1) Resistor

(a) Open

(b) Short (*)(**)

(c) Resistance increase over plus tolerance (*), to open

(d) Resistance decrease under minus tolerance, to short (*)(**)

(2) Four Terminal Resistor

(a) Open of each terminal

(b) Open of resistance material (*)(**)

(c) Short circuit across the resistive element (*)(**)

(d) Increase of resistance value (*)

(e) Decrease of resistance value (*)(**)

(f) Short circuit between two terminals of same side of the resistive element (**)

(3) Potentiometer

(a) Open

(b) Short

(c) Resistance increase over plus tolerance, to open

(d) Resistance decrease under minus tolerance, to short

(e) Increase in contact resistance of slider

(f) Change in division ratio

(4) Crystal or Crystal Oscillator

(a) Open Circuit

(b) Change in Frequency

(c) Short circuit

(d) Short circuit to case, if the case is conductive

(e) Decrease in Q

(5) Diode

(a) Open

(b) Short

(c) Short to case, if the case is conductive

(d) Leakage current

(e) Consider effect of rectifying stray ac into circuit

(f) Decrease of reverse breakdown voltage

(g) Increase of forward voltage (**)

(h) Decrease of forward voltage (**)

(6) Capacitor

(a) Open

(b) Short

(c) Increased leakage (**), to short

(d) Short to case, if the case is conductive

(e) Increased dissipation factor

(f) Increased capacitance (*)(**)

(g) Decreased capacitance (*)(**)

(7) Four Terminal Capacitor

(a) Open of each terminal

(b) Short circuit across the capacitive element

(c) Short to case, if the case is conductive

(d) Increase of capacitance (**)

(e) Decrease of capacitance (**)

(f) Increased leakage (**), to short circuit

(g) Increased dissipation factor

(h) Short circuit between two terminals of same side of the capacitive element (**)

(8) Light Emitting Diodes (LEDs)

(a) Open

(b) Short

(c) Decrease in light output at constant current

(d) Increase of leakage current

(e) Increase or decrease of forward voltage

(f) Change in LED color output

(g) Light emission below threshold voltage

(h) Light emission with reverse polarity

(i) Consider effect of rectifying stray ac into circuit

(9) Zener Diode

(a) Open

(b) Short

(c) Short to case, if the case is conductive

(d) Increase or decrease forward voltage (**)

(e) Increase or decrease reverse voltage (**)

(f) Leakage current

(g) Consider effect of rectifying stray ac into circuit

(10) Transistor (other than Field Effect Transistors)

(a) Open, each element

(b) Short, element to element and element to case, if case is conductive

(c) Leakage current, element to element and element to case, if case is conductive

(d) Increased gain (if not employed for switching) (**)

(e) Decreased gain

(f) Saturation voltage change

(g) High frequency emitter-follower oscillation

(h) Change of rise, fall, turn on, or turn off time

(i) Increase of threshold voltage

(j) Decrease of threshold voltage

(11) Field Effect Transistor

(a) Open, each element

(b) Short, element to element and element to case

(c) Leakage current, element to element and element to case

(d) Increase of forward transconductance

(e) Decrease of forward transconductance

(f) Increase of gate threshold voltage

(g) Decrease of gate threshold voltage

(h) Change of turn-on-time and turn-off time

(i) Change of static drain to source on-state resistance

(12) Thyristor

(a) Open, each element

(b) Short, element to element and element to case

(c) Leakage current, element to element

(d) Change in holding current

(e) dv/dt false turn-on effects

(13) Transformer

(a) Open primary

(b) Open secondary

(c) Turn-to-turn short, primary (**)

(d) Turn-to-turn short, secondary (**)

(e) Interwinding short (**)

(f) Winding to core short (**)

(g) Signal feed-through with winding ground points opened (inter-winding capacitance feed-through)

(h) Increase of winding resistance

(i) Increase of inductance (**)

(j) Decrease of inductance (**)

(k) Change in transfer ratio (**)

(14) Inductor

(a) Open

(b) Short

(c) Turn-to-turn short (**)

(d) Winding to core short (**)

(e) Ratio of normal signal level to saturating signal level

(f) Increase winding resistance

(g) Increase of inductance (**)

(h) Decrease of inductance (**)

(15) Relays

(a) One or more back contacts fail to open when relay is energized

(b) One or more front contacts fail to close when relay is energized

(c) One or more back contacts fail to close when relay is de-energized

(d) One or more front contacts fail to open when relay is de-energized (*)

(e) Change in timing characteristics

(f) Insulation failure, contact-to-contact, contact-to-coil, or contact to frame or ground

(g) Open, coil

(h) Increase contact resistance

(i) Increase pick-up current

(j) Decrease pick-up current

(k) Increase drop-away current

(l) Decrease drop-away current

(m) Closure of any front contact at the same time as any back contact (transient or continuous) (*)

(n) Chattering or fluttering of contacts

(o) Relay picks up if reverse polarity voltage is applied (*)

(16) Fuse

(a) Open circuit

(b) Failure to open when required (**)

(c) Increased Resistance

(17) Jumper or Jumper Posts

(a) Short circuit when required open

(b) Open circuit when required short

(c) Low resistance

(d) High resistance

(18) Optically Coupled Isolators

(a) No output

(b) Diminished band width (no response to higher frequency signals)

(c) Current transfer ratio degradation

(d) Intermittent operation

(e) Unstable detector stage amplification

(f) Increased detector stage leakage current

(g) Input to output short (**)

(h) Output stuck high

(i) Output stuck low

(j) Degradation of the isolation between input and output

(19) Surge Arrestor

(a) Open circuit

(b) Short circuit

(c) Short circuit to conductive case

(d) Change in breakdown voltage

(e) Leakage current

(20) Switch

(a) Open circuit or increased resistance, any contact

(b) Short circuit or decreased resistance, any contact

(c) Failure to Make

(d) Failure to Break

(e) Chattering or fluttering of contacts

(21) Multiple Components Connected to Common Bus

(a) Abnormal circuit configurations due to circuit openings at various points along the bus

(b) Abnormal return current paths and voltage drops due to openings at various points along the bus

(22) Connector(s)

(a) Open circuit any pin

(b) Increased resistance

(c) Short between adjacent pins or to ground (*)

(d) Leakage between pins (*)

(e) Leakage to ground (*)

(f) Wrong mechanical position

(23) PC Board Traces

(a) Short or leakage between adjacent traces (including vias, through-holes, pads, etc.) (*)

(b) Short or leakage between adjacent layers at vias, through-holes and board edges (*)

(c) Abnormal circuit configurations that could occur as a result of the opening of circuits where three or more components are connected to a common node, excluding busses which are addressed in (21). Opening of circuits implies that the trace connecting one of the components is opened without affecting the connection of the other components.

d. Integrated Circuits

(1) Integrated Circuits (including microprocessors) cannot have all of their failure modes credibly predicted due to the device complexity. The following process shall be used for analysis of integrated circuits:

(a) All hazardous failure modes related to the functionality of the specific integrated circuit shall be determined using Fault Tree Analysis and Functional Fault Tree Analysis as described in IEEE 1483-2000.

(b) For each identified hazardous failure mode, an assessment and justification shall be made to show that either:

(i) The failure mode cannot credibly occur, due to the internal architecture of the integrated circuit, or

(ii) The failure mode will be externally detected and a safe state imposed.

(c) For integrated circuits and microprocessors, the following minimum list of failures shall be considered.

(i) Incorrect or ambiguous system inputs

(ii) Inputs not present at the prescribed time

(iii) Incorrect system outputs

(iv) Outputs not present at the prescribed time

(v) System output when necessary inputs are not present

(vi) Changed memory contents

(vii) Changed clock rate

(viii) Data not current

(ix) Failure to exit from loop

(x) Arithmetic error

(xi) Sign error

(xii) Entry to or exit from a routine at the wrong time

(xiii) Illegal entry to a routine

(xiv) Improper execution of instructions

(xv) Skipping of program segments

(xvi) Failure to reset upon command

(xvii) Failure to halt upon command

(xviii) Latent faults

(xix) Common cause faults

(xx) Transient faults

(xxi) Intermittent Faults

(xxii) Other faults particular to the specific technology

(xxiii) High frequency oscillation on any pin

e. Special Components

(1) Failure Modes of Special Components can be considered “not credible” and the relevant failure modes of those components may be excluded from the safety analysis. Satisfactory justification must be provided in order for these failure modes to not be considered credible. As a minimum, the justification must include the following:

(a) Theoretical explanation of any inherent physical properties or characteristics.

(b) Evidence of compliance that the component has been properly produced (e.g., compliance with recognized quality standards and any special manufacturing techniques/instructions required).

(c) Explanation of any special mounting arrangements or other precautions.

(d) Evidence that the failure mode will not occur as a result of component ratings (e.g., component must be de-rated, even under failure conditions, for use in the circuit).

(e) Results of tests to demonstrate fail-safe behavior of the component under adverse conditions such as adverse electrical and environmental conditions.

(f) Evidence of previous experience of reliance on the component for inherent fail-safety.

(2) Special components must be clearly identified as special safety components on schematics and assembly drawings.

(3) Generally Accepted Special Components

The following components have been generally accepted within the industry as having specific failure modes that can be considered “not credible”:

(a) Metallized film resistor, MIL Type manufactured to Specification MIL-PRF-55182 or MIL-PRF-39017 (e.g., RNC/RNR/RNN/RLR60, RNC/RNR/RNN/RLR65, and

RNC/RNR/RNN/RLR70) may increase in resistance but will not decrease in resistance.

(b) Wire wound resistors, MIL Type, manufactured to Specification MIL-R-26E (e.g., RW/RWR-79), used in circuits in which their maximum dissipation does not exceed 10% of rated power, may decrease in resistance but will not increase in resistance except for a possible abrupt change to a value of 500 kilohms or higher. Note that the power dissipation limit must be maintained even in the event of failure of other components. If this is not the case, the described resistance characteristic does not apply.

(c) Wire wound resistors, MIL Type RWR-71, manufactured to Specification MIL-R-39007B, used in circuits in which their maximum dissipation does not exceed 10% of rated power (including fault conditions), will not vary in resistance more than ±5%. This acceptance characteristic requires in addition that (a) the resistors be mounted in a 4-terminal configuration which checks integrity of lead connection to external circuitry (b) leads are formed under controlled conditions (c) the mechanical stability of resistor mounting is assured by suitable supports and tie downs.

(d) Capacitors, other than electrolytic type or units built up of separate capacitance elements connected in parallel and subject to loss of internal connections, will substantially retain the original capacitance value while the dielectric and structure are intact. However, film capacitors will exhibit an increase in capacitance if moisture penetrates the foil. This is always accompanied by an increase in dissipation factor and a decrease in insulation resistance. The increase in capacitance is about 10%. Then, if an increase in capacitance is a safety problem, a different type of capacitor, or a hermetically sealed unit should be used. The specification for the unit should call for 100% inspection of the enclosure.

(e) Except for the above, two terminal capacitors may in all cases open, short and increase in leakage and dissipation. Four-terminal capacitors, properly installed, may be considered not to cause an unsafe or non-revealing failure when they fail open circuit.

(f) For Vital Relays built according to Manual Parts 6.1 Recommended Shelf Type Vital Relays, and 6.2 Recommended Plug-In Vital Relays, silver/carbon to silver contacts will not weld (stick). Therefore, a silver/carbon to silver front contact will always be open when the relay is in the de-energized position.

(g) For Vital Relays built according to Manual Parts 6.1 and 6.2, biased neutral relays will not operate on reversed energy up to 50 times the value of relay working current, nor will they remain in the energized position if energy is reversed.

(h) Relays conforming to CENELEC EN 50205 may assume the failure mode of "Closure of any front contact at the same time as any back contact (transient or continuous)" is not-credible.

(i) Connector pins or adjacent PC Board traces conforming to the creepage and clearance requirements for reinforced insulation as specified in CENELEC EN50124-1, or complying with the following criteria may assume the failure mode of short to adjacent pins/traces is "not-credible":

(i) Minimum creepage spacing between pins or traces on outer layers of PC Boards is 0.250 in (6.35 mm)

(ii) Minimum creepage spacing between conformal coated traces is 0.100 in (2.54 mm)

(iii) Minimum spacing between traces on the same interior layer of PC Boards is 0.100 in (2.54 mm)

(iv) For PCB components connected to isolated (floating) power supplies where no wires connected to that isolated circuitry leave the enclosure (i.e., are not exposed to the possibility of high voltage transients), minimum creepage spacing between pins or traces on outer layers of PC Boards is 0.050 in (1.27 mm)

(v) For PCB components connected to isolated (floating) power supplies where no wires connected to that isolated circuitry leave the enclosure (i.e., are not exposed to the possibility

of high voltage transients), minimum creepage spacing between conformal coated traces is 0.025 in (0.64 mm)

(vi) For PCB components connected to isolated (floating) power supplies where no wires connected to that isolated circuitry leave the enclosure (i.e., are not exposed to the possibility of high voltage transients), minimum creepage spacing between traces on the same interior layer of PC Boards is 0.025 in (0.64 mm)

(4) Other Component Failure Mode Considerations

The following considerations may be used in analyzing component failure modes:

(a) Resistors conforming to the following criteria may assume the failure modes of short circuit and decrease in resistance are “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(b) The body shall have no hollows.

(c) Creepage and clearance distances at each end of the component shall fulfill the requirements for conductor separation as identified in this Manual Part.

(d) The coating shall be cement or enamel.

(e) The body shall be constructed of a non-conductive material, even at the highest temperature fault conditions within the ambient operating temperature range per Manual Part 11.5.1 Recommended Environmental Requirements for Electrical and Electronic Railroad Signal System Equipment.

(f) The coating shall be of a non-conductive material, even at the highest temperature fault conditions within the ambient operating temperature range per Manual Part 11.5.1.

(g) For wirewound resistors, the component shall have only 1 layer.

(h) For wirewound resistors, short circuited turns are possible to be eliminated by wire coatings and/or physical separation between turns.

(i) The resistance shall be limited to the lowest possible value.

(5) Four terminal resistors conforming to the following criteria may assume the failure mode of resistance material open circuit is “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) Component must be constructed such that if a fault occurs causing interruption of the resistance material, at least one of the four connecting terminals will open.

(b) (b) The circuitry external to the four terminal resistor shall react in a failsafe manner in response to open terminal(s).

(6) Four terminal resistors or four terminal capacitors conforming to the following criteria may assume the failure mode of a short circuit between two terminals on the same side is “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) The two terminals on each side of the components shall be connected independently to the component.

(7) Capacitors conforming to the following criteria may assume the failure mode of increased leakage is “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) The component shall be designed for high voltage operation related to maximum operating voltage

(b) The component shall have Class Y1 specification per IEC 60384-14 and self-healing properties at the working source impedance and over the working voltage range. Ceramic Class Y1 capacitors are excluded because ceramic dielectrics are not self-healing and can have leakage and shorting failures modes.

(8) Capacitors (except electrolytic types) which can demonstrate that plate area, distance between plates, or dielectric constant cannot significantly change may assume the failure modes of increase or decrease in capacitance are “not-credible” provided the criteria in Section I.2.e.(1) are also met.

(9) Adjustable and non-adjustable inductors and adjustable or non-adjustable transformers conforming to the following criteria may assume the failure modes of short circuits

between windings, layers, turns, and body (including the core) are “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) There shall be only 1 layer of turns separated by grooves in the body or by sufficient insulation.

(b) The turns, windings, and connections shall be securely fastened.

(c) Creepage and clearance distances between exposed conductors shall fulfill the requirements for conductor separation as identified in this Manual Part.

(d) Power dissipation. shall be limited sufficiently, even under failure conditions, to prevent internal carbonization.

(10) Non-adjustable inductors and non-adjustable transformers conforming to the following criteria may assume the failure modes of an increase or decrease of inductance in any winding are “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) The magnetic core shall be constructed such that no significant change in reluctance of the magnetic path can occur (For example, core materials fracturing or cracking could decrease inductance).

(b) All criteria listed in Section I.2.e.(9) above.

(11) Non-adjustable transformers conforming to the following criteria may assume the failure mode of a change in transfer ratio is “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) All criteria listed in I.2.e.(9) and I.2.e.(10) above

(12) Optocouplers conforming to the following criteria may assume the failure mode of a short circuit input to output is “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) Creepage and clearance distances shall fulfill the requirements for conductor separation as identified in this Manual Part.

(b) The construction of the component shall be robust and stable

(c) Power dissipation, even under fault conditions, shall be limited sufficiently to prevent internal carbonization

(d) Dielectric strength conforming to Manual Part 11.5.1 Recommended Environmental Requirements for Electrical and Electronic Railroad Signal System Equipment is satisfied.

(13) The gain of a transistor is dependent on doping levels, thickness of the junction(s), and lifetime of charge carriers. For a given temperature, the gain should only decrease with time.

(14) Fuses conforming to the following criteria may assume the failure mode of failure to open when required is “not-credible” provided the criteria in Section I.2.e.(1) are also met:

(a) The fuse and its holder shall be physically constructed and mounted so as to prevent the occurrence of a parallel short circuit.

(b) Means shall be provided to prevent the use of an incorrectly rated fuse.

(c) Means shall be provided to prevent the use of a fuse with self-resetting or self-healing capability.

(15) The forward voltage of a diode or Zener diode is dependent on non-variable characteristics of the p-n junction (charge carrier density, Boltzmann’s constant, electron charge) and should therefore be constant for a given temperature.